TSMC-02-1398

March 22, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/754,835 01/09/04

Min-Hsiung Chiang

METHOD TO REDUCE A CAPACITOR DEPLETION PHENOMENA

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date  3/25/04

U.S. Patent 6,661,043 to Huang et al., "One-Transistor RAM Approach for High Density Memory Application," discusses a new method for the creation of a 1T RAM cell.

U.S. Patent 6,555,430 to Chudzik et al., "Process Flow for Capacitance Enhancement in a DRAM Trench," discusses methods forming a trench region of a trench capacitor structure having increase surface area.

U.S. Patent 6,420,226 to Chen et al., "Method of Defining a Buried Stack Capacitor Structure for a One Transistor RAM Cell," discloses a process for fabricating a buried stack capacitor structure, to be used in a one transistor, RAM cell.

U.S. Patent Application Publication US 2002/0094697 A1 to Leung et al., "DRAM Cell having a Capacitor Structure Fabricated Partially in a Cavity and Method for Operating Same," discusses a memory system that includes a dynamic random access memory (DRAM) cell including an access transistor and a capacitor structure fabricated in a semiconductor substrate.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

OIPE MAR 2 9 2004 PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-1398	10/754,835
Applicant: Min-Hsiung Chiang	
Filing Date: 01/09/04	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6661043	12/9/03	Huang et al.	257	243	3/27/03
	6555430	4/29/03	Chudzik et al.	438	243	11/28/00
	6420226	7/16/02	Chen et al.	438	238	12/12/01

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

US Patent App. Publication US 2002/0094697 A1 to Leung et al., Pub. Date 7/18/02, US Class 438/766, filed 11/2/01.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.